OFFICE OF THE DIRECTOR OF NATIONAL INTELLIGENCE

IARPA Trusted Integrated Chips (TIC) Program

LEADING INTELLIGENCE INTEGRATION

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INTELLIGENCE ADVANCED RESEARCH PROJECTS ACTIVITY (IARPA)

Outline

- Introduction
- TIC Program Details
- Summary

Introduction

Office of the Director of National Intelligence

IARPA Mission and Method

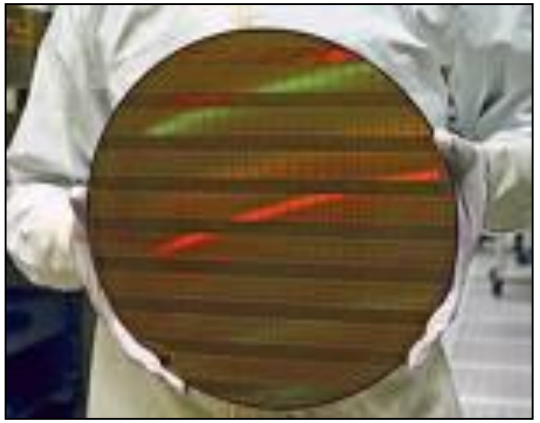
IARPA's mission is to invest in high-risk/high-payoff research to provide the U.S. with an overwhelming intelligence advantage

- **Bring the best minds to bear on our problems**
  - Full and open competition to the greatest possible extent
  - World-class, rotational Program Managers
- **Define and execute research programs that:**
  - Have goals that are clear, measureable, ambitious and credible
  - Employ independent and rigorous Test & Evaluation
  - Involve IC partners from start to finish
  - Run from three to five years
  - Publish peer-reviewed results and data, to the greatest possible extent

TIC Program Details

TIC Program Vision

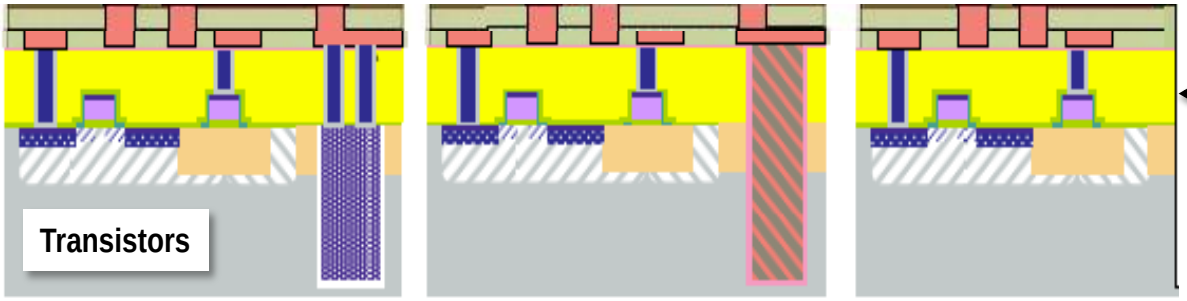
- Ensure the U.S. Intelligence Community can obtain the highest performance possible in integrated circuit chips.
- Ensure capability, performance, and security of designs.
  - Designs not compromised with malicious circuitry.
  - Design intellectual property protected.
- Demonstrate split-manufacturing of chips using an advanced untrusted* FEOL (Front End of Line) foundry and a trusted* BEOL (Back End of Line) foundry.



*Trust certification per current DMEA accreditation.

TIC Split-Manufacturing Process

Basic Functions (FEOL)

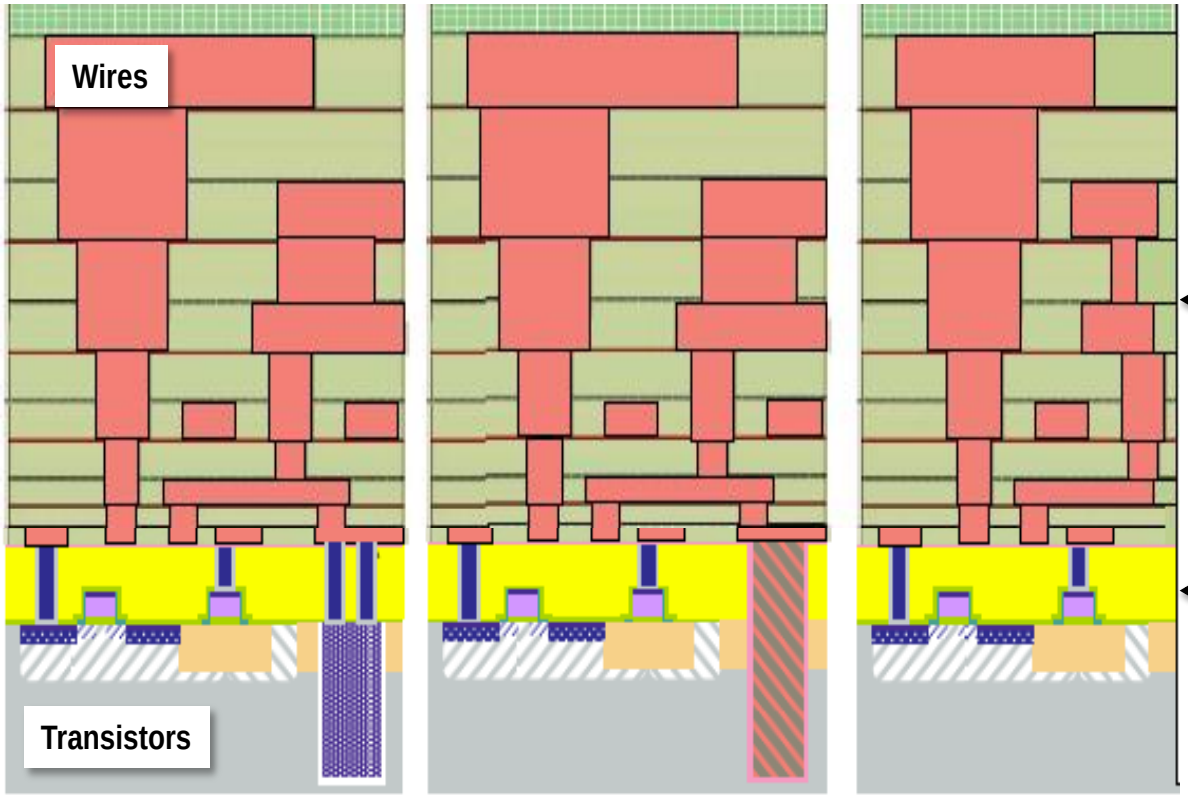


CMOS Transistors + Low Level Metallizations (Untrusted)

TIC Split-Manufacturing Process

Application Functionality (BEOL)

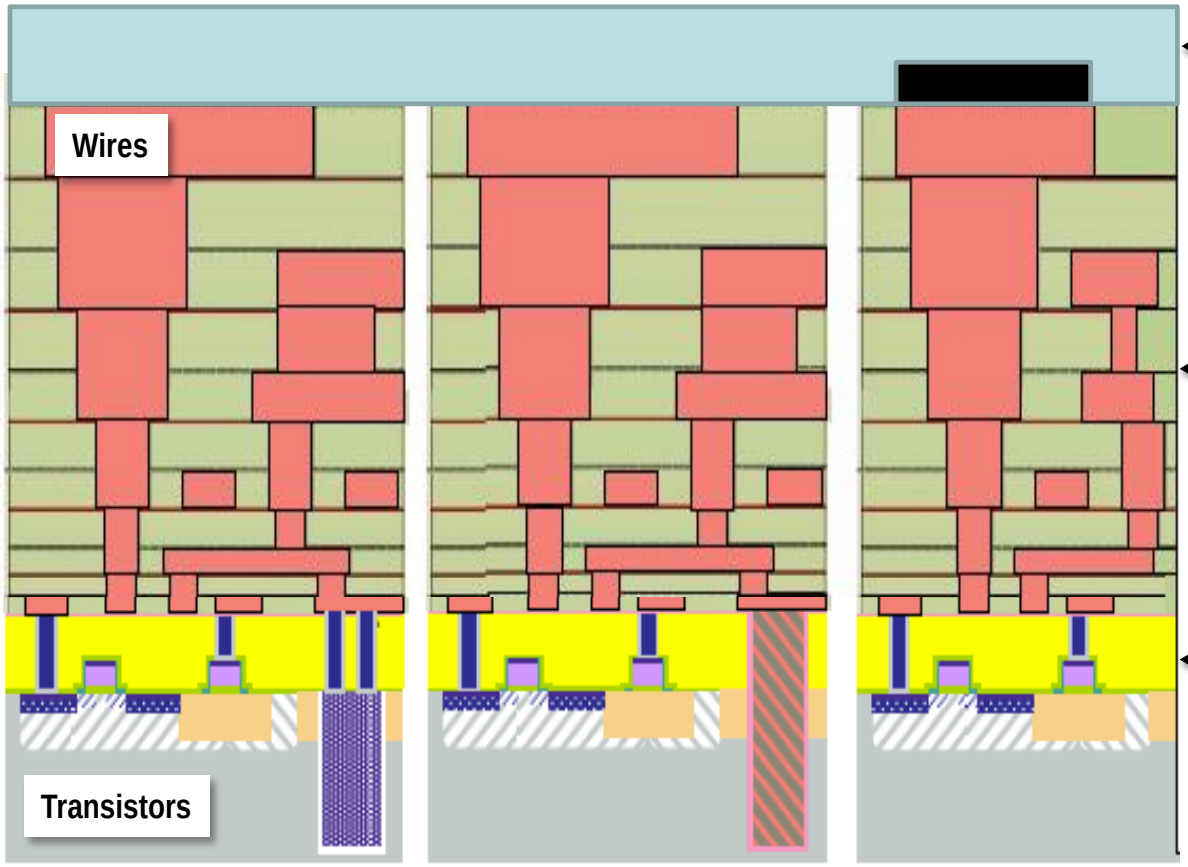
Basic Functions (FEOL)



← Metallizations (Trusted)

← CMOS Transistors + Low Level Metallizations (Untrusted)

TIC Split-Manufacturing Process



Application Functionality (BEOL)

Basic Functions (FEOL)

MtM: MEMS, Photonics, Add'l chips (US Performer)

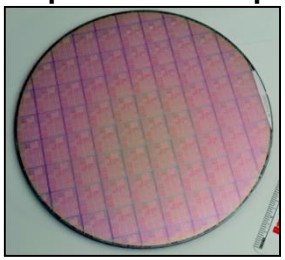
Metallizations (Trusted)

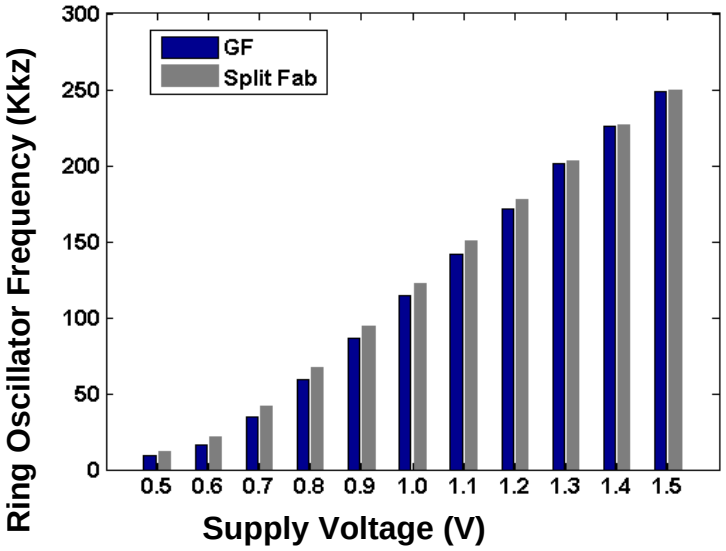
CMOS Transistors + Low Level Metallizations (Untrusted)

TIC 130 nm Wafer and Test Chips

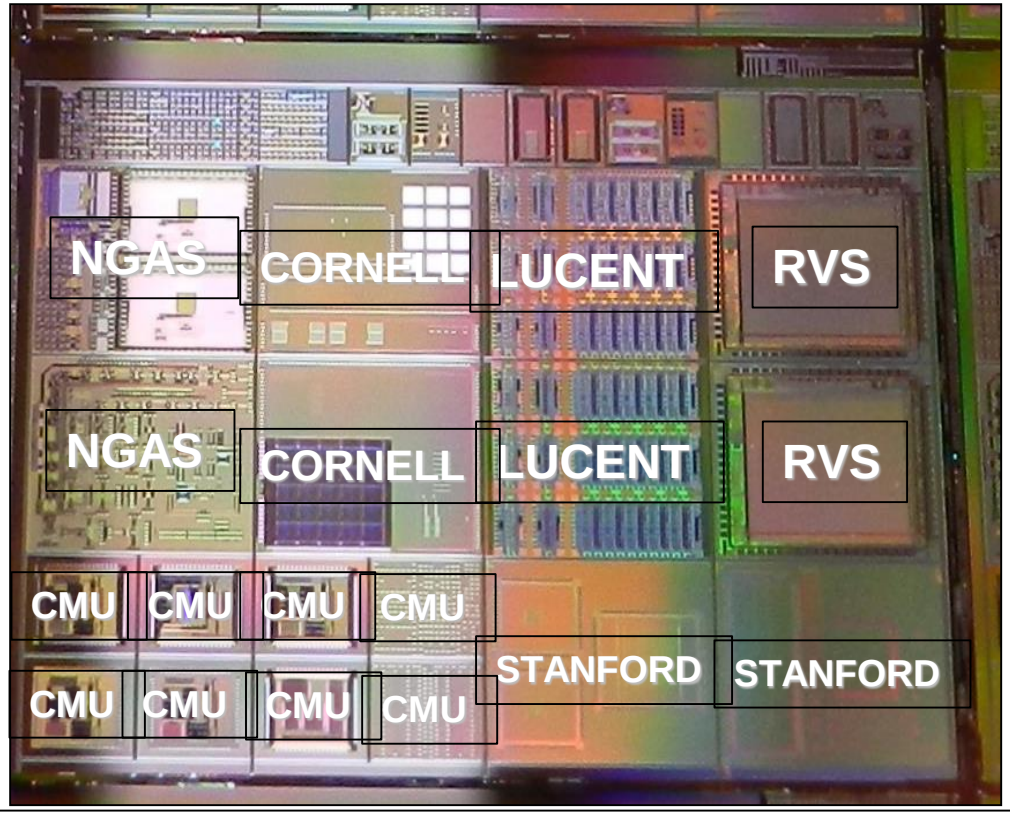
Split-manufactured integrated circuits in six different electronic families produced are fully functional and within process specification.

TIC 130nm
MPW-1 200 mm Wafer
Global Foundries / IBM





No significant difference in electrical performance.

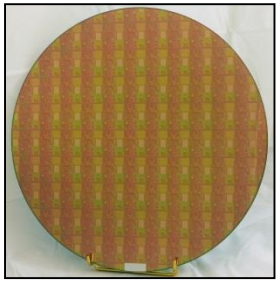


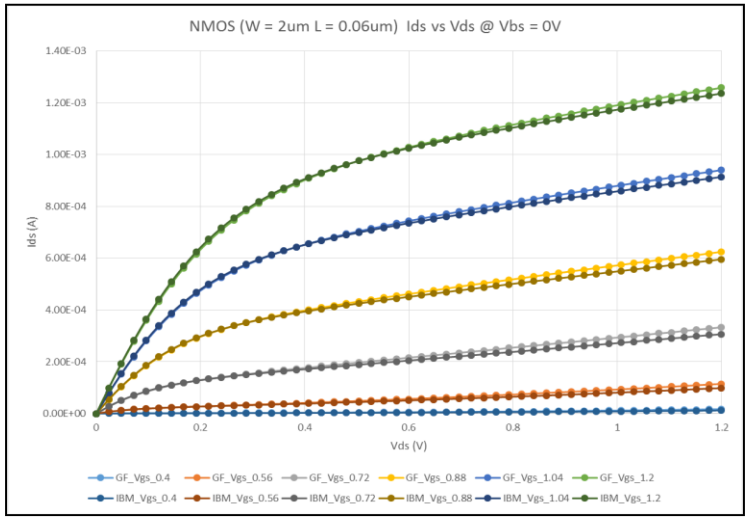
IARPA multi-user test chip April 2013 fabricated jointly between Global Foundries (Singapore) and IBM (Burlington, VT).

TIC 65 nm Wafer and Test Chips

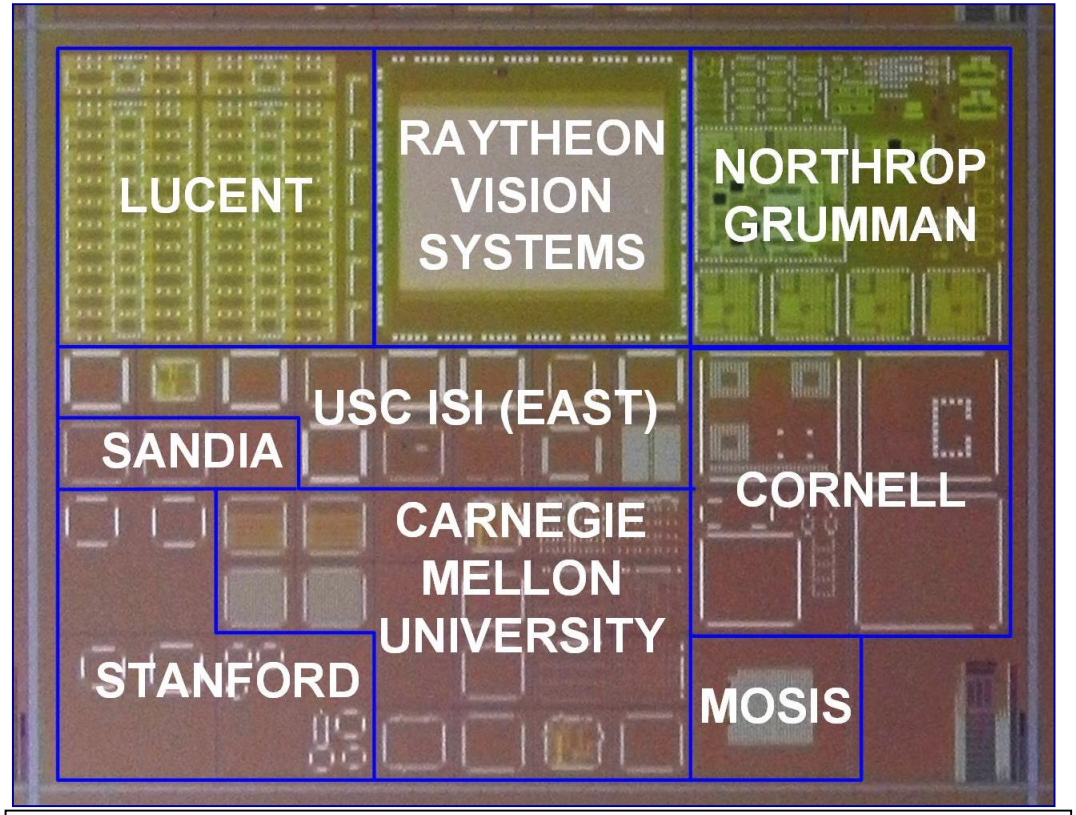
Split-manufactured integrated circuits show working circuits and are within process specification

TIC 65nm
MPW-1 300 mm Wafer
Global Foundries / IBM





No significant difference in electrical performance

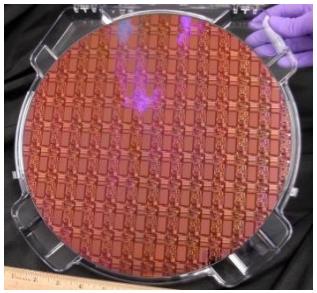


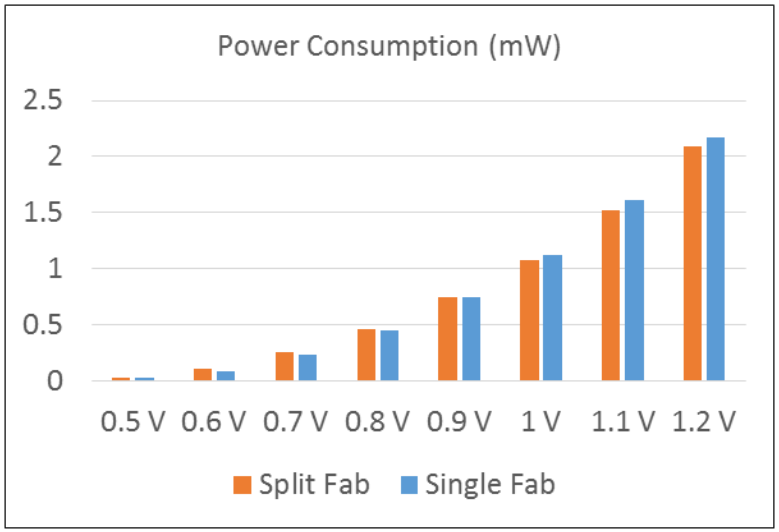
IARPA multi-user test chip April 2014 fabricated jointly between Global Foundries (Singapore) and IBM (East Fishkill)

TIC 28 nm Wafer and Test Chips

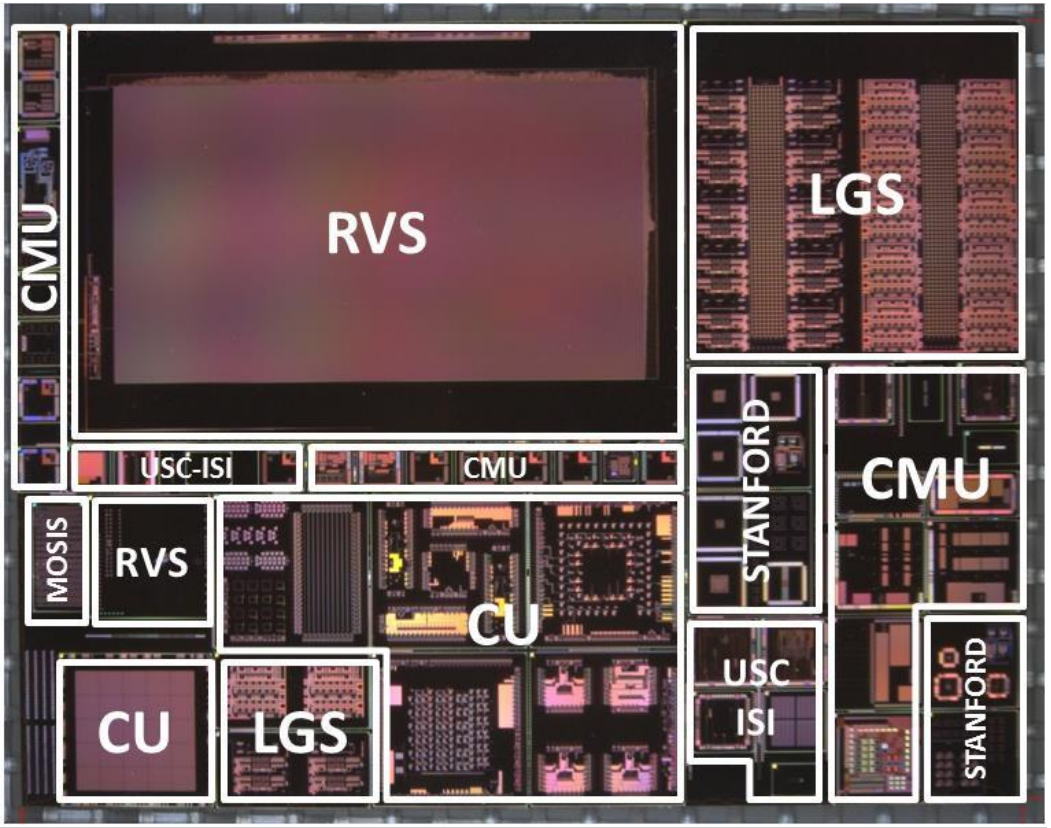
Split-manufactured integrated circuits with working circuits and are within process specification

TIC 28nm
MPW 300 mm Wafer
Samsung / Samsung





Power consumption for multiplier circuit.
No difference between split fab & reference.



IARPA multi-user test chip December 2015 fabricated jointly between Samsung (Korea) and Samsung (Austin).

Phase 2 Final Program Results

Metrics		OY 2 (18 mo)	CMU	Cornell	LGS/Bell Labs	RVS	Stanford
Technology Node		28 nm node	28 nm node	28 nm node	28 nm node	28 nm node	28 nm node
Circuit Complexity (# of transistors)	Digital	>1M	>3M	82.5M	~15M	1000M	>1M
	Analog/Mixed Signal	>1K	>10K	>30K	~14K	>>1K	na
Split-Fabrication Yield		>75%	100%	95%	78%	96%	95%
Speed		>85%	100%	90%	86%	*83%	95%
Power Dissipation		<120%	105%	104%	100%	*92%	105%

CMU = Carnegie Mellon University
RVS = Raytheon Vision Systems

* For Phase 2, the speed and power curves for split and non-split devices overlap.

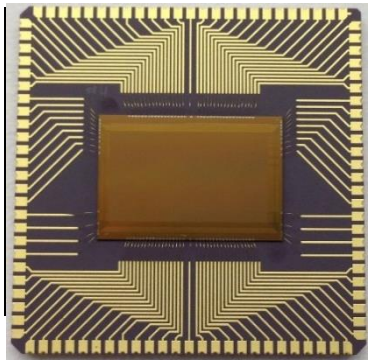
TIC Circuit Example

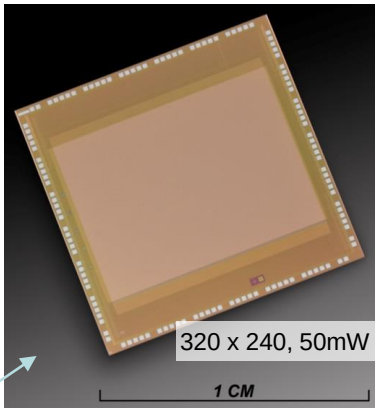
Raytheon Vision Systems

Raytheon

Goal: Develop low size, weight and power electro-optical sensors by designing ROICs at advanced CMOS process nodes.

Imager built using 28 nm CMOS



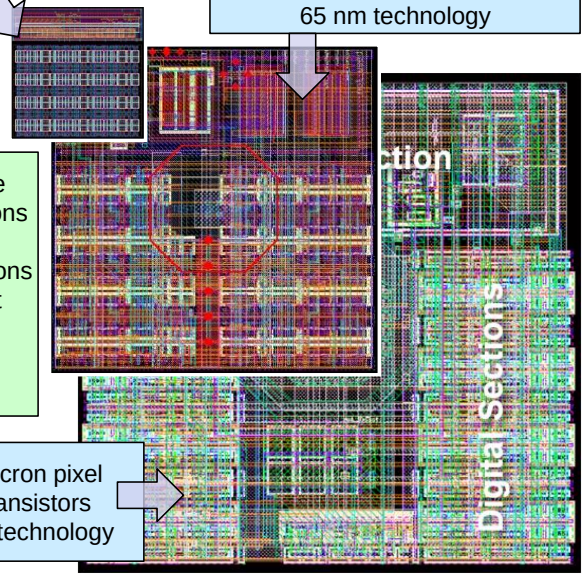


Raytheon's QVGA IR Imager, 65k:1 dynamic range, built on 65nm CMOS

A 9 micron pixel, using offshore 28 nm processing enables 65k:1 high-contrast night vision. An 800x600 imager could be the width of a pencil eraser, contain ¾ billion transistors, and run 2 hours on a set of AA batteries.

9 micron pixel
1100 transistors
28 nm technology

25 micron pixel, 850 transistors
65 nm technology



To-scale comparisons of 3 generations of 16 bit infrared imaging pixels

37.5 micron pixel
540 transistors
130 nm technology

Summary

TIC Program Major Accomplishments

	Phase 1a	Phase 1b	Phase 2
Process Node	130nm / 130nm	65nm / 65nm	28nm / 28nm
FEOL	GLOBAL FOUNDRIES	GLOBAL FOUNDRIES	SAMSUNG
BEOL	IBM	IBM	SAMSUNG
Accomplishments / Results	Successfully demonstrated: •Split at low level metal (MET1) •FEOL and BEOL by two different foundries •Five technologies	Successfully demonstrated: ▪ Split-fab at < 90nm ▪ Obfuscation/ITAR ▪ Split at low level metal (MET2) ▪ Five technologies	Successfully demonstrated: ▪ Split-fab at advanced node ▪ Full split-fab (split at contact) ▪ Five technologies

Questions?