Evolving the Electronics Resurgence Initiative (ERI 2.0)

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Briefing prepared for NDIA

April 21, 2021

MTO
MICROSYSTEMS TECHNOLOGY OFFICE

(U) MTO's core mission is the development of high-performance, intelligent microsystems and next-generation components to enable dominance in national security C4ISR, EW, and DE applications

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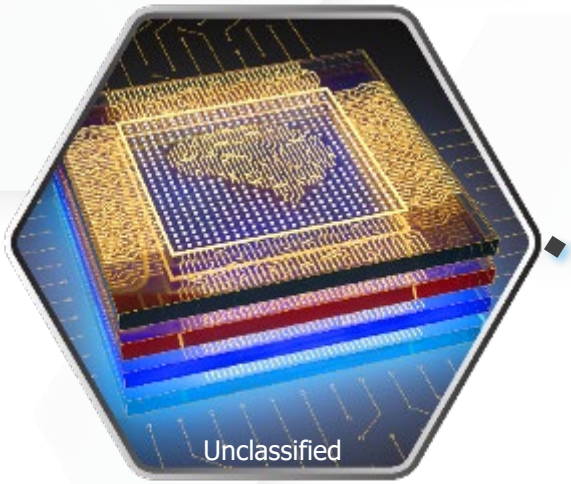
(U) The effectiveness, survivability, and lethality of these systems depends critically on microsystems

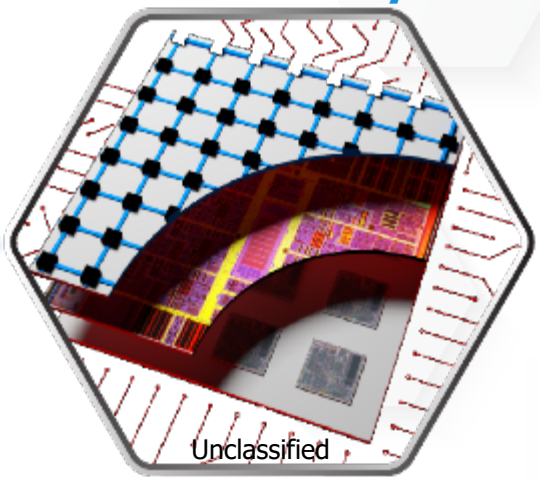
(U) C4ISR: Command, Control, Communications, Computer, Intelligence, Surveillance, and Reconnaissance

MICROSYSTEMS TECHNOLOGY OFFICE

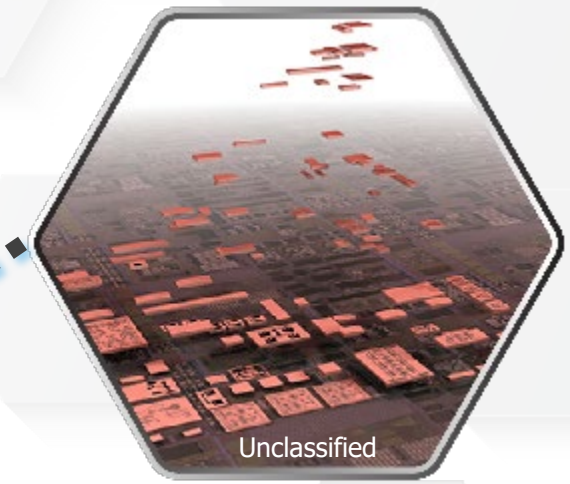
(U) Embedded Microsystem Intelligence / Localized Processing



(U) Microsystem Integration for Functional Density & Security



(U) Next Gen Front-End Technologies for Electromagnetic Spectrum Dominance

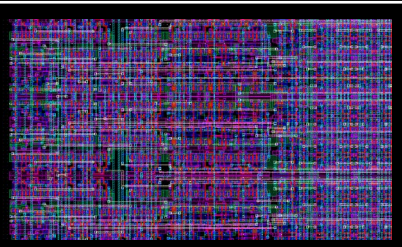


(U) Disruptive Defense Microsystem Applications

In 2017, DARPA launched the Electronics Resurgence Initiative (ERI) in response to several industry trends

Increasing Reliance on Advanced Electronics

Exploding Microsystem Complexity



Offshore Movement of Advanced Capabilities

Emergence of Hardware Security Threats

- Our greatest technical challenges are intrinsically "**dual-use**" ones that depend on and demand working with industry
- Our national security cannot not be assured without **a strong domestic microelectronics industry**
- There has been **convergence of the goals** and concerns of DoD with that of the US industrial base

The Electronic Resurgence Initiative today

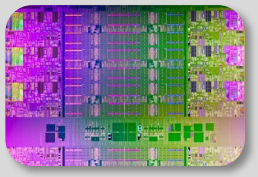
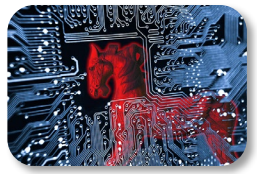
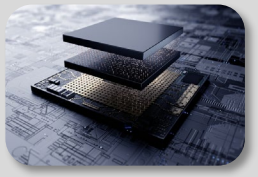
PURPOSE: Address domestic capability in semiconductor manufacturing and development

U.S. Semiconductor Industry:

- **2001**: Nearly **30** semiconductor firms manufactured leading-edge chips
- **2018**: Only **5** leading-edge manufacturers located in Taiwan, Korea, and the U.S.
- **2019**: **80%** of semiconductor foundries and assembly/test ops are concentrated in Asia

(Data from SIA 2020 Report

ERI is collaboratively innovating a 4th wave of electronics progress

1. Increasing information processing density and efficiency 	4. Mitigating the skyrocketing costs of electronics design 
2. Accelerating innovation in AI hardware to make decisions at the edge faster 	5. Overcoming security threats across the entire hardware lifecycle 
3. Overcoming the inherent throughput limits of 2D electronics 	6. Revolutionizing communications (5G and beyond) 

COLLABORATION:

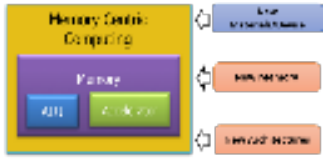
- **6** of top 10 Semiconductor Sales Leaders*
- **9** of top 10 Engineering Universities*
- **All 5** top Defense Contractors*

Intel **Qualcomm** **Xilinx** **Samsung** **NVIDIA** **Micron**

Raytheon Technologies **Lockheed Martin** **Boeing** **Northrop Grumman** **BAE Systems**

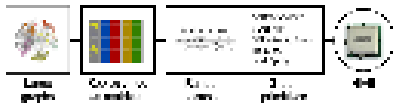
* Based on 2018 sales data and U.S. News reports

Defense Industrial Base participants are critical to driving some of ERI's biggest accomplishments



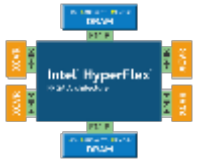
FRANC

New materials for combined memory and computation



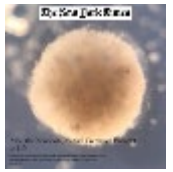
HIVE

Fast, small, random, global memory access across a flat, low-latency network



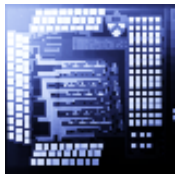
Domestic Foundries

ICs fabricated in Intel 22nm node for DIB applications



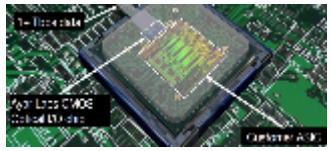
L2M

Continuous learning for autonomous navigation with 25x less forgetting



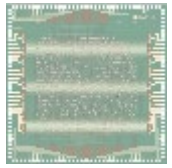
PEACH

Photonic reservoir AI for compact, low-latency edge hardware



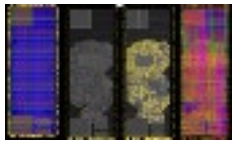
PIPES

TA1B employed LM, NG, and Raytheon to explore DoD applications



3DSoC

Utilize 3rd dimension & carbon nanotubes for 50x compute performance



IDEA

Cadence's integration of machine learning into design tools

AISS

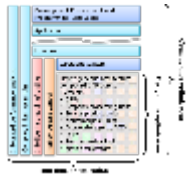
Synopsys' effort to incorporate security features into chip designs

SSITH

Mitigation of hardware vulnerabilities with minimal performance impact

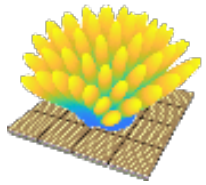
GAPS

Rapid partitioning of existing legacy code for secure transactions



DSSOC

Power and cost efficient domain-specific architectures



MIDAS

Demo of world's first mmW digitally beamformed array

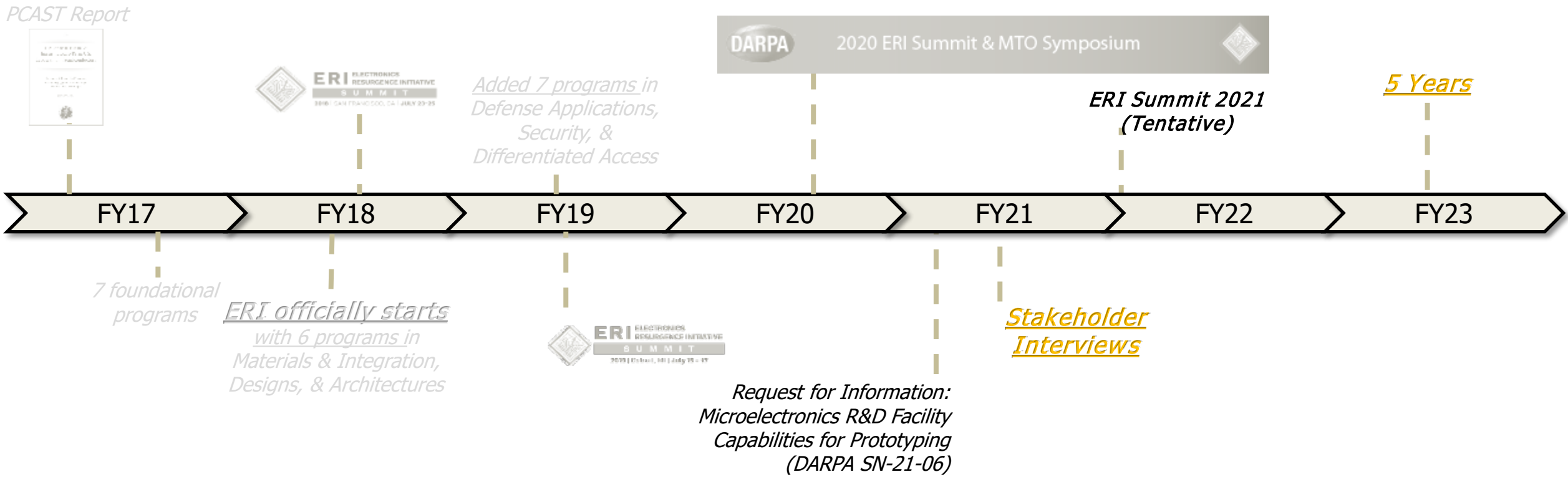
Other Programs

T-MUSIC
SDH
POSH
SHEATH

All images courtesy of DARPA

ERI timeline

Currently 2.5 years into a 5 year program



What's next?

NDAA authorizes new models to support innovation and access

FY21 NDAA

SEC. 9903. DEPARTMENT OF DEFENSE

The DoD may –

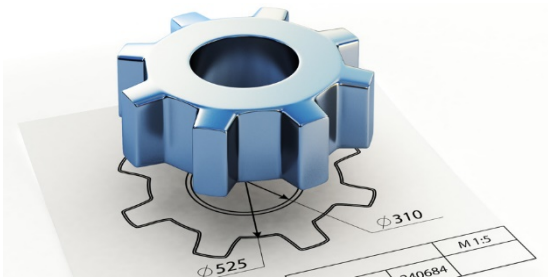
- *establish a national network for microelectronics research and development— (A) to enable the laboratory to fabrication transition of microelectronics innovations in the United States; and (B) to expand the global leadership in microelectronics of the United States.*

SEC. 276. MICROELECTRONICS AND NATIONAL SECURITY.

The DoD (including DARPA) shall deliver –

- *(14) A plan for **increasing commercialization** of intellectual property developed by the Department of Defense…*
- *(15) An assessment of the feasibility, usefulness, efficacy, and cost of (A) developing a **national laboratory** exclusively focused on the research and development of microelectronics… and (B) incorporating...access to funding resources, fabrication facilities, design tools, and shared intellectual property [for early-stage microelectronics startups]…*
- *(16) The development of multiple models of **public-private partnerships** to execute the strategy, including in-depth analysis of establishing a semiconductor manufacturing corporation…*

https://share.america.gov/how-bill-becomes-law/



https://www.egofabrication.com/prototype-development.html

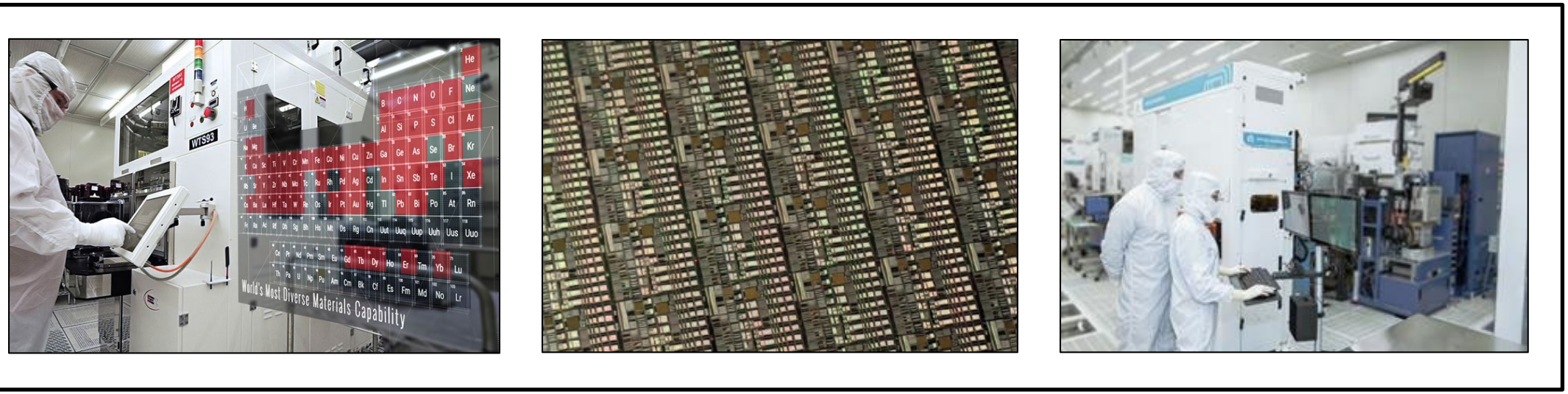
Current assumptions informing ERI 2.0 planning

- Maintaining US supremacy in semiconductor technologies over the long-term demands national investment in disruptive technologies
- Scaling of transistors is unlikely to persist much further, and in any case will not drive future microelectronic innovation
- Future microelectronics will instead be tied to the ability to design, fabricate, and test and model the performance of complex 3D assemblies composed of heterogeneous microelectronic technologies
- Lab-to-fab capability represents an opportunity to accelerate and re-shore future manufacturing

A path for leadership in the next generation of microelectronics

Problems

1. Need to accelerate the pace of microelectronics innovation for both US industry and defense
2. On-shore fabrication is limited and fractured, hampering U.S. innovation in this fast-emerging technology area
3. Existing EDA tools cannot adequately address emerging development nor support full-digital design and emulation



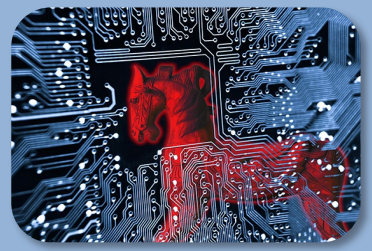
Possible approach

1. R&D to support re-establishing US leadership in microelectronics (ERI 2.0 Research)
2. On-shore facility with advanced processes and software tools (ERI 2.0 Lab-to-Fab Infrastructure)

ERI 2.0 may expand investment in dual use research

Current Areas of Emphasis

Overcoming security threats across the entire hardware lifecycle



- EDA based technology
- Inspection and supply chain based technology

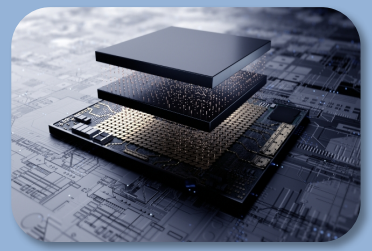
Mitigating the skyrocketing costs of electronics design

- Foundry-portable IP
- Design tools with ML capability

Revolutionizing communications (5G and beyond)

- Power efficient digital arrays
- Techniques for secure communications

Overcoming the inherent throughput limits of 2D electronics

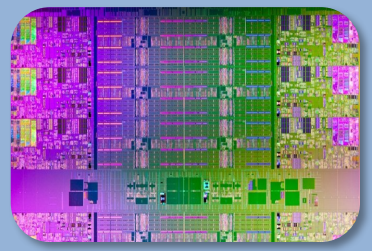


- Heterogeneous electronics with Si-like back-end
- Integration of photonics / optics

Accelerating innovation in AI hardware to make decisions at the edge faster

- Alternative / approximate computing
- AI / ML integrated with HW

Increasing information processing density and efficiency



- New computing architectures, devices, and materials
- Quantum-inspired algorithms

Potential New Areas

Manufacturing complex 3D microsystems

- ML / AI automated tools
- Desktop assembly

Developing electronics for harsh environments

- Radiation-hardened electronics
- High-temperature electronics

Two distinct development timeframes could benefit from investment

Near-term National Strategy
Continuing advanced CMOS scaling

- Leading edge manufacturing technologies (e.g. 3-nm CMOS)
- New computing concepts (e.g. compute-in-memory)
- Chip-level and wafer-level packaging and integration
- Domestic and quantifiably assured manufacturing

Image courtesy of IMEC

Image courtesy Kvdh

Potential future:
U.S.-based facility such as authorized in FY21 NDAA (e.g. NSTC)

Development of and access to mature technology

Longer-term DARPA Focus
Augment, extend or displace CMOS

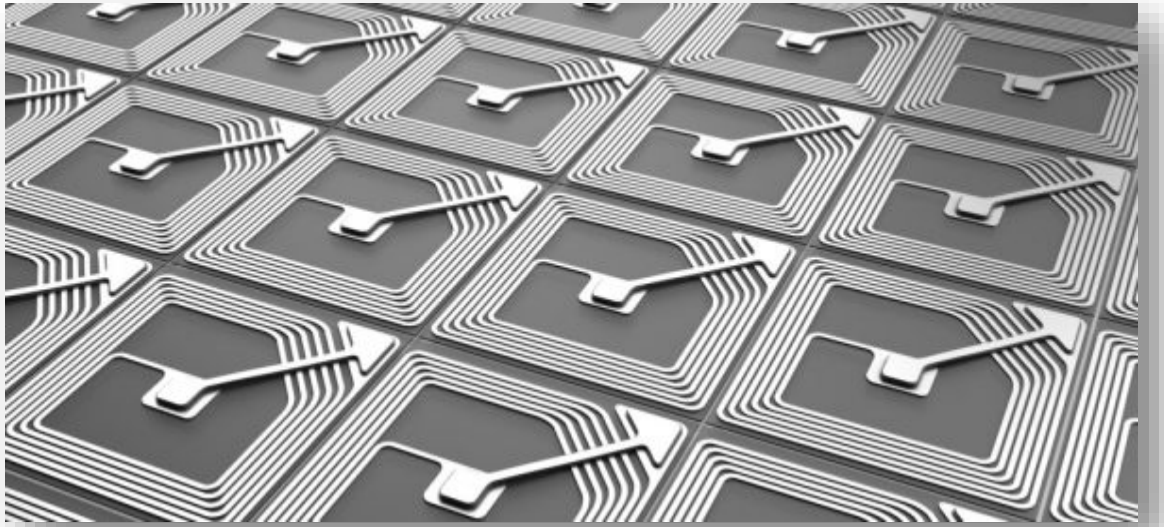
- Overcoming security threats
- Mitigate design costs
- Overcoming the limits of 2D
- Faster decisions at the edge
- Increase processing efficiency
- Revolutionizing communications
- *Harsh environments*
- *Manufacturing complex 3D microsystems*

Potential future:
Research and infrastructure

Enhancing disruptive microelectronics

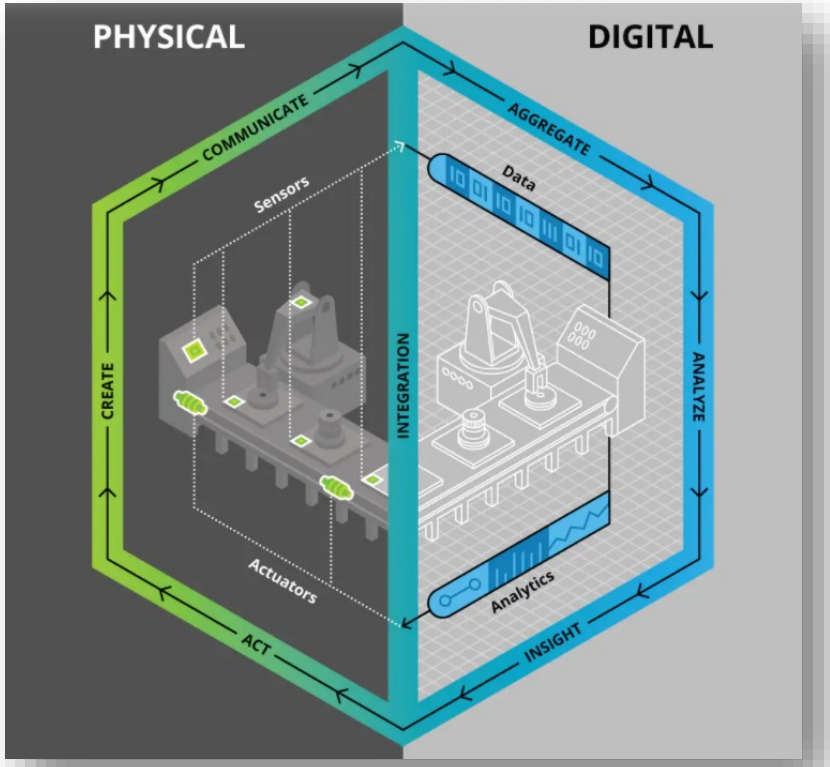
Potential ERI 2.0 Lab-to-Fab focus areas

Manufacture / assembly of 3DHI microelectronics



https://www.sunchemical.com/wp-content/uploads/2019/11/Nanosilver-600x259.jpg

Software tools to design/simulate/emulate 3DHI microelectronics

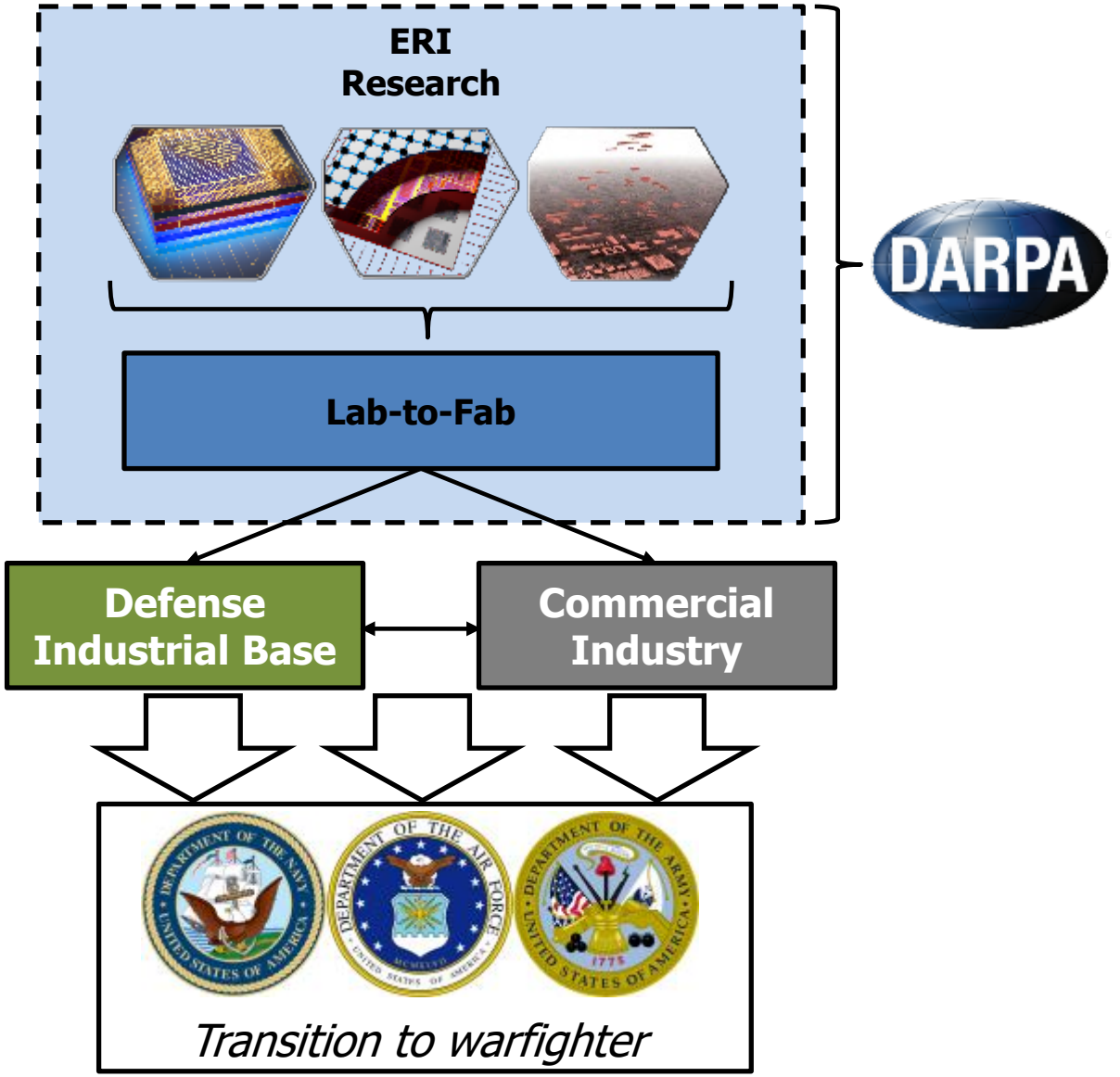


https://www2.deloitte.com/us/en/insights/focus/industry-4-0/digital-twin-technology-smart-factory.html/

Targeted infrastructure may de-risk new technologies

Key Concepts under consideration

- **Customers**: University, start-up, and major corporation innovators
- **Infrastructure:** One or more user facilities focused on manufacturing-relevant prototyping activities
  - Vertical integration, from idea to system
  - Easy facility access (co-location, tele-access)
- **Funding**: Sustainable operating model supplemented by consistent Federal support
- **Staff:** Permanent staff available to support R&D access to design, manufacturing, and packaging tools
- **Transition Support**: Resources and connections to support access to follow-on capital, to include domestic commercial, and defense industry companies



ERI 2.0 tentative development plan

Stakeholder Outreach
Gather community feedback

- *Prototyping Infrastructure RFI*
- *SIA & NDIA leader meetings*
- *Address public-private partnership models*
- *Interview and survey community*

Jan 2020 – July 2020

Define Plans
Engage community in planning

- *Possible new research areas*
- *Workshops (tentative)*
- *Coordinate with other agency plans*

Aug 2021 – Oct 2021

Launch
Describe plans to community

- *Workshops (tentettive)*
- *ERI Summit (tentative)*

Oct 2021

Key questions for feedback

- **What new, dual-use research areas should ERI incorporate, with high impact for national security?**
- **Should any of the existing research focus areas be de-emphasized?**
- **How can we ensure the ability of NDIA members to securely innovate for national security in broadly accessible facilities?**
- **What mechanisms would be more useful to accelerate the transition of new technologies?**

www.darpa.mil